Amendments to the Specification:

Page 1, beginning at line 22, replace with the following paragraph:

In many portable power applications, a voltage that exceeds the battery voltage is required to operate certain circuits such as a video display. DC-DC converters are switching-type regulators that can be used to generate higher output voltages from a battery voltage. The output voltage is typically provided to a load circuit by varying the conduction time that is associated with a controlled device. Example controlled devices include transistors, gate-turn-on (GTO devices), thyristors, diodes, as well as others. The frequency, duty cycle, and conduction time of the controlled device is varied to adjust the average output voltage to the load. Typical DC-DC converters are operated with some sort of oscillator circuit that provides a clock signal. The output voltage of the converter is also determined by the oscillation frequency associated with the clock signal.

Page 2, beginning at line 5, replace with the following paragraph:

At the start of each cycle of the oscillator, the SR latch is set and transistor Q_1 is turned on via driver circuit DRV_1. Amplifier A_3 produces a sense voltage (V_{SNS1}) by sensing the switching current from transistor Q_1 via sense resistor ~~R_{NSN1}~~ R_{SNS1}. . The signal (V_{SUM}) at the non-inverting input of the PWM comparator (A_2) is determined by the switch current via V_{SNS1}, summed together with a portion of the oscillation ramp signal. Amplifier A_1 is an error amplifier that provides an error signal (V_{ERR}) by evaluating the drive current (I_{LED}) via transistors Q_2 and resistor R_{SNS2}. The PWM comparator (A_2) resets the SR latch and turns off transistor Q_1 when the sum signal (V_{SUM}) reaches the level set by the error signal (V_{ERR}). Thus, amplifier A_1 and driver circuit DRV1 set the peak current level to keep the drive current (I_{LED}) in regulation. Resistor R_{SET} is adjusted to change the peak current level via a reference circuit (REF) and amplifier A_1.

Page 4, beginning at line 12, replace with the following paragraph:

Capacitor C_{IN} is coupled between the input voltage (V_{IN}) and ground. Resistor R_{SET} is coupled between the RAMPGEN and ground. RAMPGEN is arranged to provide a ramp voltage (V_{RAMP}) with a known slope when enabled. Ramp voltage V_{RAMP} corresponds to ground when RAMPGEN is disabled via signal ~~RES~~ ENR. REF CKT is arranged to provide a voltage reference (V_{REF}). Inductor L is selectively coupled to ground through transistor switch circuit T_{SW} when transistor switch circuit T_{SW} is active, and coupled to the stack circuit through Schottky diode D_S when transistor switch circuit T_{SW} is inactive. The stack circuit is coupled between Schottky diode D_S and ground. Capacitor C_{OUT} is coupled in parallel with the stack circuit to minimize ripple in the output voltage (V_{OUT}). Feed-forward circuit FFCKT is arranged to sense the voltage (V_{SW}) associated with the non-input side of inductor L and provides a signal to an input of latch circuit LATCH. Comparator COMP is arranged to compare ramp voltage V_{RAMP} to reference voltage V_{REF} and provide a comparison signal (V_{COMP}) to another input of latch circuit LATCH. One output of latch circuit LATCH is arranged to provide signal ~~RES~~ ENR. Another output of latch circuit LATCH is arranged to selectively activate transistor switch circuit T_{SW} via driver circuit DRV and signal V_{GATE}. Start up circuit START UP is arranged to force signal V_{GATE} during a start-up sequence (when EN is active) such that inductor L is charged and the latch is initialized to an appropriate condition via comparator COMP and the feed-forward circuit.

Page 5, beginning at line 8, replace with the following paragraph:

Ramp generator RAMPGEN is illustrated as a current source (CS) that has an output coupled to a capacitor (C_R), and an input that is coupled to resistor RSET. Transistor switching circuit T_{SW} is configured to short capacitor (C_R) to ground when signal ~~RES~~ ENR is active such that the ramp is reset to a known value before each ramp cycle begins. Current source CS provides a current (I_{MATH}) to capacitor C_R such that the capacitor charges at a constant rate. The charging rate is adjusted by changing the magnitude of current I_{MATH}, which is adjusted by resistor R_{SET}.

Page 5, beginning at line 15, replace with the following paragraph:

The output current (I_{OUT}) is adjusted by changing a value associated with resistor R_{SET}, which in turn adjusts the slope of ramp voltage V_{RAMP}. The slope of ramp voltage V_{RAMP} controls the on-time (T_{ON}, see FIGURE 3) associated with transistor switch circuit T_{SW}, which in turn controls the charging of inductor L. For example, comparator COMP controls the gate voltage (V_{GATE}) via driver circuit DRV and latch circuit LATCH such that transistor switching circuit T_{SW} is disabled when the ramp voltage (V_{RAMP}) exceeds the reference voltage (V_{REF}).